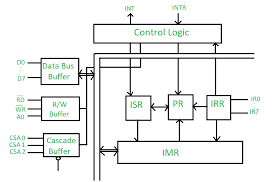
***8259 PROGRAMMABLE INTERRUP CONTROLLER***

**When we need multiple sources, we need to use an external device called as Priority Interrupt Controller (PIC). PIC helps to increase the Interrupt Handling Capacity of the Microprocessor. 8259A is the commonly used PIC which can easily help in handling Non-Vectored Interrupt of 8086-INTR.**

**FEATURES OF 8259**

1. **Programmable Interrupt used to work with 8086 and 8085.**
2. **Can Handle Edge as well as Level Triggered Interrupt**
3. **Flexible Priority Structure**
4. **Interrupts Can be Masked Individually**
5. **Vector Address of Interrupt is Programmable**
6. **Single 8259 can handle 8 Interrupts while cascaded configuration of 1 Master 8259. Similarly 8 Slave 8259 can handle 64 Interrupts**

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| --- | --- |
| **BLOCK** | **INFORMATION** |
| **Data Bus Buffer** | * **Bi-Directional Buffer used to interface the internal data bus of 8259 with any external data bus.** * **Used to send read and control signals** * **Used to read interrupt type from the 8259** |
| **Read Write Logic** | * **Used to accept RD,WR,Ao,CS Signal** * **Used to control Data flow on Data Bus** * **Holds Initialization Command Words (ICWs) and Operational Commands Words(OCWs)** |
| **Comparator or Cascade Buffer** | * **Used in cascade mode operation** * **CAS2, CAS1, CAS0:  Output for Slave and Input for Master.**   **Using these 3 Lines there are 8 Possible Interrupts (23=8)**  **The Master Sends Address of the Slave on this lines**  **The Slaves read the address on these lines.**   * **SP/EN :   EN – Used to Enable the Buffer in Buffered Mode**   **SP – Functions as Output Line in Non Buffered Mode** |
| **Interrupt Request Register** | * **IRR – 8 Bit Register having 1-Bit for each interrupt lines IR7-IR0** * **Interrupt request occurs and the corresponding bit is set in the IRR** |
| **Interrupt Mask Register** | * **IMR- 8 Bit Register storing Masking Information of Interrupt IR7-IR0** * **This is written by the Programmer** |
| **In Service Register** | * **InSR - 8 Bit Register storing info about Interrupt Request being serviced** |
| **Priority Resolved** | * **Examines IRR,IMR,InSR and examines which interrupt has the highest priority of them all and send it to the micro-processer** |
| **Control Logic** | * **INT Output Signal connected to the INTR of Microprocessor** * **Also has the INTA input connected to the INTA of the Microprocessor** * **Also used to control the remaining blocks** |

**PIN CONFIGURATION of 8259**

|  |  |  |
| --- | --- | --- |
| **PIN** | **NUMBER** | **INFORMATION** |
| **Vcc** | **28** | **+5V Power Supply** |
| **GND** | **14** | **Ground** |
| **CS** | **1** | **Chip Select – Low on this pin enables RD and WR Communication** |
| **WR** | **2** | **Write – Low on this command enables to accept command words from CPU** |
| **RD** | **3** | **Read - Low on this command enables to release status onto data bus** |
| **D7-D0** | **4-11** | **Bidirectional Data Bud for data transfer** |
| **CASo-CAS2** | **12,13,15** | **Cascade Lines to control multiple 8259A structure** |
| **SP/EN** | **16** | **Slave Program or Enable Buffer**  **EN – Used to Enable the Buffer in Buffered Mode**  **SP – Functions as Output Line in Non Buffered Mode** |
| **INT** | **17** | **Interrupt Pin goes high when a valid interrupt request is asserted and is used to interrupt the CPU** |
| **IR0-IR7** | **18-25** | **Interrupt Request is asserted by pin going from low to high** |
| **INTA** | **26** | **Enable 8259 vector data into data bus by a Interrupt Acknowledgement** |
| **Ao** | **27** | **AO Address Line acts in conjunction of CS,WR,RD, and is used to decipher various command words** |

**END OF INTERRUPT**

**There are 3 different ways of sending END OF INTERRUPT command and they are as follows:**

|  |  |
| --- | --- |
| **Automatic EOI** | **No command needed here**  **In the 3rd INTA cycle corresponding bit in the InSR is reset** |
| **Non Specific EOI** | **Command is send to 8259 at the end of service routine**  **This would clear the bit of the currently serviced interrupt in InSR** |
| **Specific EOI** | **Command is send to 8259 at the end of service routine**  **This would clear the bit of the specified serviced interrupt in InSR** |

**OPERATION MODES**

**There are 2 different ways of Operating Modes of 8259 and they are as following**

|  |  |
| --- | --- |
| **Interrupt Driven** | **8259 interrupts processor with the INT Pin whenever it encounters a interrupt** |
| **Polled Mode** | **Here the INT mode is not used and checks the interrupt request by issuing the poll command. The micro-processor reads contents of 8259 and issues the poll command. During read operation provides polled words and sets the InSR bit of highest active interrupt** |

**PRIORITY MODES**

1. **Fully Nested Modes**
   1. **Default Mode of 8259**
   2. **Fixed Priority Mode**
   3. **IR0 – Highest and IR7 – Lowest**
2. **Special Fully Nested Modes**
   1. **Used for Master 8259 in cascading mode.**
   2. **The priority for the same are same as Fully Nested Modes**
   3. **Consider a large system that uses cascading 8259 where the interrupt level of each interrupt has to be considered. An interrupt input to the slave causes the slave to place an interrupt request to the master and on one of Master’s Input**
   4. **Interrupts to the same slave will not be recoganized and thus disabling further interrupts. This can be prevented using SFNM**
3. **Rotating Priority Mode**
   1. **Automatic Rotation Mode**
      1. **Preferred when multiple interrupts have the same priority**
      2. **After a device requests service, then it gets the lowest priority**
      3. **All other priorities rotates subsequently**
   2. **Specific Rotation Mode**
      1. **Here the user can fix the priorities**
4. **Special Mask Mode**
   1. **8259 disables interrupt requests lower or equal to the interrupt which is currently under service. SMM allows interrupts of all levels except one currently in service**
5. **Poll Mode**
   1. **Here INT line of 8259 is disabled**
   2. **Microprocessor gives Poll Command to 8259 using OCW3 and in return gets a Poll Word and then the service of interrupt takes place**
   3. **Helps when we need expand number of interrupts more than 64**
6. **Buffered Mode**
   1. **SP/EN becomes low during the INTA cycle and this is used to enable the buffer**